

PHS 205 Digital Circuit Design

4 cr. [DII]

Instructor: TBA **Office:** location **Phone:** (978) 542-extension
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Section	Time	Room	Final Exam
nn	Days and times	location	Date and time

Catalog description:

This course is an introduction to logic design and digital circuit fundamentals. Topics include: binary systems, Boolean algebra, combinatorial and sequential circuit analysis and design, and fundamental building blocks of modern computers, such as multiplexers, decoders, counters and registers. Hands-on laboratory activities and team projects are required to apply learned theory in design, simulation and implementation of digital circuits using current computer aided-design software and hardware tools. Three lecture hours and three hours of scheduled laboratory per week.

Pre- or Co-requisite: MAT 220, or MAT 110 or equivalent.

Goals:

This course introduces students to logic design and digital circuit fundamentals. Specific goals are:

- CG01: to gain a basic understanding of the digital logic devices and digital circuit fundamentals
- CG02: to become familiar with basic logic operations using different analysis and design tools
- CG03: to develop a firm understanding of logic principles as applied to integrated circuits
- CG04: to develop a working knowledge of the components in a computer system

Objectives:

Upon successful completion of this course the student will have demonstrated the ability:

- CO01: to manipulate numeric information in different forms, e.g., different number systems, signed and unsigned integers, different coding systems, e.g., ASCII, Unicode, Gray code, and BCD.
- CO02: to apply Boolean algebra theory to manipulate simple Boolean expressions.
- CO03: to use different tools for the analysis and the design of small combinational circuits, e.g., truth tables, K-maps.
- CO04: to use different tools for the analysis and the design of small sequential circuits, e.g., timing diagrams, state transition diagrams, etc.
- CO05: to analyze and design larger and more complex circuits using SSI and MSI devices
- CO06: to analyze and design larger and more complex circuits using programmable logic devices (PLDs), e.g., PROMs, PLAs, PALs, and FPGAs.
- CO07: to use state-of-the-art computer aided-design software and hardware tools in design, simulation and implementation of a variety of digital circuits
- CO08: to work in a team of 2 or 3 members on a project that may involve more complex design goals.

Program Outcome vs. Course Objectives matrix

Program Objective (condensed form)	CO01	CO02	CO03	CO04	CO05	CO06	CO07	CO08
PO-A: apply knowledge of computing and math	✓	✓	✓	✓	✓	✓	✓	✓
PO-B: analyze a problem and define its computing requirements			✓	✓	✓	✓	✓	✓
PO-C: design, implement and evaluate applications			✓	✓	✓	✓	✓	✓
PO-D: function effectively in teams to accomplish a common goal								✓

Program Objective (condensed form)	CO01	CO02	CO03	CO04	CO05	CO06	CO07	CO08
PO-E: professional, ethical, and social responsibilities								
PO-F: communicate effectively with a range of audiences								
PO-G: local and global impact of computing on people and society								
PO-H: need for continuing professional development						✓	✓	
PO-I: use current techniques, skills, and tools	✓	✓	✓	✓	✓	✓	✓	✓
PO-J: apply theory and principles to model and design systems		✓	✓	✓	✓	✓	✓	✓
PO-K: apply design and development principles in constructing software								
PO-L: apply knowledge of computing and mathematics appropriate to the discipline	✓	✓	✓	✓	✓	✓	✓	✓
note - full statements of the Program Outcomes (program objectives) for the Computer Science Major can be found in the document <i>Computer Science Major Program Educational Objectives and Program Outcomes</i> on the Assessment page of the Computer Science Major (cs.salemstate.edu)								

Topics:

- Data Representation in Digital Systems **AR1(5)**
AR2(1)
 - Digital Systems
 - Positional Number Systems
 - Representation of Fixed-Point Unsigned Numbers
 - Representation of Fixed-Point Signed Numbers
 - Conversion Between Numbers of Different Representations
 - Binary Addition and Subtraction
 - Binary Codes

- Boolean Algebra, Logic Functions and Logic Gates **AR1(5)**
 - Basic Definition of Boolean Algebra
 - Basic Theorems and Properties of Boolean Algebra
 - Boolean Functions and Logic Expressions
 - Using Truth Table to Define a Logic Function
 - Canonical and Standard Logic Expressions
 - Other Logic Operations and Logic Gates

- Gate-Level Minimization **AR1(5)**
 - Karnaugh Maps for Simplification of Logic Functions
 - Four-Variable K-Map
 - Product-of-Sums Simplification
 - Don't-Care Conditions
 - NAND and NOR Implementation
 - Other Two-Level Implementations
 - Exclusive-OR Function
 - Hardware Description Language

- Combinational Logic **AR1(7)**
 - Combinational Circuit Analysis Procedure
 - Implementation of Combinational Logic Functions
 - Combinational Circuit Design Procedure
 - Ripple-Carry Adder/Subtractor with External Logic for Subtraction

- Decimal Adder
- Binary Multiplier
- Magnitude Comparator
- Dynamic Characteristics of Combinational Logic Circuits
- HDL Models of Combinational Circuits

- Combinational MSI Modules and Programmable Logic Devices **AR1(5)**
AR4(1)
 - Multiplexer
 - Decoder/Demultiplexer
 - Encoder
 - Read-Only Memory (ROM)
 - Programmable Logic Array (PLA)
 - Programmable Array Logic (PAL)
 - Complex Programmable Logic Devices (CPLDs)
 - Field-Programmable Gate Arrays (FPGAs)

- Synchronous Sequential Logic **AR1(7)**
 - General Model of Sequential Circuits
 - Storage Elements: Latches
 - Storage Elements: Flip-Flops
 - Clocked Sequential Circuit Analysis Procedure
 - Analysis of Clocked Sequential Circuits
 - Sequential Circuit Design Procedure
 - Synthesizable HDL Models of Sequential Circuits
 - State Reduction and Assignment
 - Design of a Finite State Machine

- Sequential MSI Modules **AR1(4)**
AR4(1)
 - Sequential Programmable Devices
 - Registers
 - Shift Registers
 - Ripple Counters
 - Synchronous Counters
 - Other Counters
 - HDL for Registers and Counters

- Laboratory Activities and Team Projects using Computer Aided-Design Software and Hardware Tools **AR1(7)**
AR4(1)
 - Lab Exercise 1: Introduction to Simulation and Rapid Prototyping with FPGAs
 - Lab Exercise 2: Digital Logic Gates
 - Lab Exercise 3: Simplification of Boolean Functions
 - Lab Exercise 4: Combinational Circuits
 - Lab Exercise 5: Code Converters
 - Lab Exercise 6: Design with Multiplexers
 - Lab Exercise 7: Adders and Subtractors
 - Lab Exercise 8: Flip-Flops
 - Lab Exercise 9: Sequential Circuit Analysis
 - Lab Exercise 10: Counters
 - Lab Exercise 11: Shift Registers
 - Lab Exercise 12: Serial Addition
 - Team Project 1: Parallel Adder and Subtractor
 - Team Project 2: Design of a Sequence Detector
 - Team Project 3: Design of a Digital Clock
 - Team Project 4: Design of a Traffic Light Controller
 - Team Project 5: Design of an Elevator Controller

This course lays the groundwork for several junior and senior level courses in computer architecture and organization, real-time computer interfaces, and microcomputing systems. Students are exposed to design problems that involve trade-offs in terms of

speed, cost and complexity. Students are introduced to computer aided-design tools such as schematic capture, HDL description and simulation.

Students are evaluated using 5-10 homework assignments, 5-10 laboratory activities, one mid-term examination and a final examination. Student grade will be determined using the following approximate weights: final examination - 25%, midterm examination - 25%, laboratory activities - 15%, team projects – 15%, and written homework - 20%.

Course Objective / Assessment Mechanism matrix

Assessments	Homework	Laboratory Activities	Examinations	Team Projects
CO01	✓	✓	✓	✓
CO02	✓	✓	✓	✓
CO03	✓	✓	✓	✓
CO04	✓	✓	✓	✓
CO05	✓	✓	✓	✓
CO06	✓	✓	✓	✓
CO07	✓	✓	✓	✓
CO08				✓

Bibliography:

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- Brown, Stephen; Vranesic, Zvonko, **Fundamentals of Digital Logic with VHDL Design with CD-ROM, First Edition**, McGraw-Hill, 2004
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- Holdsworth, Brian; Woods, Clive, **Digital Logic Design, Fourth Edition**, Newnes, 2002.
- Jain, R.P., **Modern Digital Electronics, Fourth Edition**, Tata McGraw Hill, 2010
- Jin, Lan; Hatfield, Bo, **Computer Organization: Principles, Analysis & Design, First Edition**, Tsinghua University Press, 2004.
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- Langholz, Gideon; Kandel Abraham; Mott, Joe L., **Foundations of Digital Logic Design, First Edition**, World Scientific, 1998
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- Marcovitz, Alan B., **Introduction to Logic Design, Second Edition**, McGraw Hill, 2005.
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- Wirth, Niklaus, **Digital Circuit Design for Computer Science Students: An Introductory Textbook, First Edition**, Springer, 1995

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“Salem State University assumes that all students come to the University with serious educational intent and expects them to be mature, responsible individuals who will exhibit high standards of honesty and personal conduct in their academic life. All forms of academic dishonesty are considered to be serious offences against the University community. The University will apply sanctions when student conduct interferes with the University primary responsibility of ensuring its educational objectives.” Consult the University catalog for further details on Academic Integrity Regulations and, in particular, the University definition of academic dishonesty.

The Academic Integrity Policy and Regulations can be found in the University Catalog and on the University website (http://catalog.salemstate.edu/content.php?catoid=13&navoid=1295#Academic_Integrity). The formal regulations are extensive and detailed - familiarize yourself with them if you have not previously done so. A concise summary of and direct quote from the regulations: "Materials (written or otherwise) submitted to fulfill academic requirements must represent a student's own efforts". *Submission of other's work as one's own without proper attribution is in direct violation of the University's Policy and will be dealt with according to the University's formal Procedures. Copying without attribution is considered cheating in an academic environment - simply put, **do not do it!***

University-Declared Critical Emergency Statement:

In the event of a university-declared emergency, Salem State University reserves the right to alter this course plan. Students should refer to www.salemstate.edu for further information and updates. The course attendance policy stays in effect until there is a university-declared critical emergency.

In the event of an emergency, please refer to the alternative educational plans for this course, which will be distributed via standing class communication protocols. Students should review the plans and act accordingly. Any required material that may be necessary will have been previously distributed to students electronically or will be made available as needed via email and/or Internet access.

Equal Access Statement:

"Salem State University is committed to providing equal access to the educational experience for all students in compliance with Section 504 of The Rehabilitation Act and The Americans with Disabilities Act and to providing all reasonable academic accommodations, aids and adjustments. **Any student who has a documented disability requiring an accommodation, aid or adjustment should speak with the instructor immediately.** Students with Disabilities who have not previously done so should provide documentation to and schedule an appointment with the Office for Students with Disabilities and obtain appropriate services."

Note: This syllabus represents the intended structure of the course for the semester. If changes are necessary, students will be notified in writing and via email and the class website.